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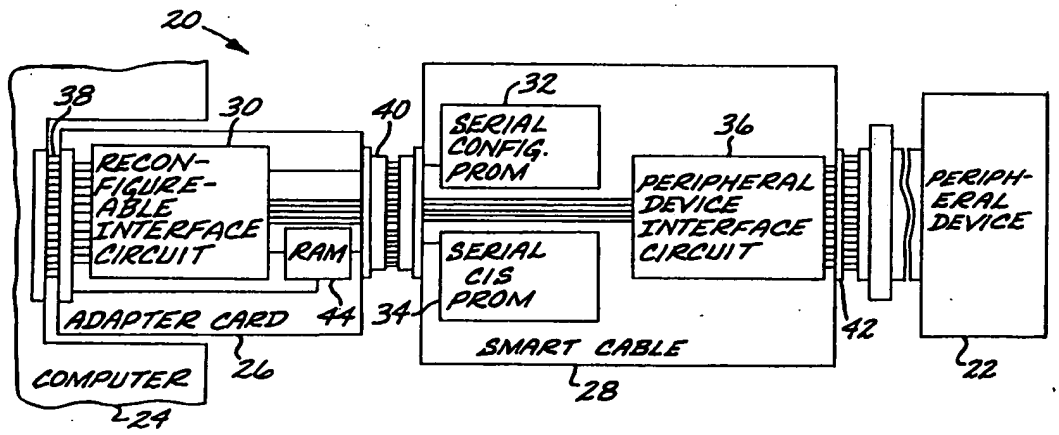
(54) Title: RECONFIGUREABLE INTERFACE BETWEEN A COMPUTER AND PERIPHERAL DEVICES



(57) Abstract

An apparatus (20) used to interface a peripheral device (22) to a computer (24) has an adapter card (26) that plugs into the computer (24) and a smart cable (28) that plugs into the adaptor card (26) at one end and the peripheral device (22) at the other. The adapter card (26) includes a reconfigureable interface circuit (30) that is in communication with the computer (24) when the adapter card (26) is connected to the computer (24). The smart cable (28) includes a first memory (32) containing configuration information for the reconfigureable interface circuit (30), and a second memory (34) containing adapter card information structure information for the reconfigureable interface circuit (30). The two memories are accessible by the reconfigureable interface circuit (30) when the smart cable (28) is connected to the adapter card (26). The smart cable (28) further includes a peripheral device interface circuit (36) communicating with the reconfigureable interface circuit (30) and with the peripheral device (22) when the smart cable (28) is connected to the adapter card (26) and the peripheral device (22) is connected to the smart cable (28). Connectors between the computer (24) and the adaptor card (26), the adapter card (26) and the smart cable (28), and the smart cable (28) and the peripheral device (22) are also provided.

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Description

Reconfigureable Interface Between A Computer and Peripheral Devices

Technical Field

This invention relates to computer systems, and, more particularly, to the connection of peripheral devices to computers.

Background Art

One of the important features of computers is their ability to connect to, exchange information with, and control (and be controlled by) various accessories. In some cases, accessories are internal to the computer. In other cases, due to size or other requirements, the accessories are external to the computer, and are termed "peripheral devices".

In the conventional approach for interfacing a portable computer to a peripheral device, a special-purpose PCMCIA card plugs into the computer. The interface may be split into two portions, the PCMCIA card itself and an outboard assembly, commonly termed a "dongle". The PCMCIA card contains a portion of the electronics required to interface the computer to the peripheral device, as well as the logic required to create an intermediate bus-like interface to communicate between the PCMCIA card and the dongle. The remaining interface electronics, as well as the interface to the intermediate bus, are placed in the dongle. The outboard assembly is usually in the form of a cable that plugs into the PCMCIA card at one end and the peripheral device at the other end. The PCMCIA card and the outboard assembly cable are special-purpose devices useful only with the peripheral device for which they are designed.

When the computer user wishes to add a

new peripheral device to the capability of the computer, the PCMCIA card and the outboard assembly cable are purchased along with the other structure and software of the peripheral device. In some instances, such as the modem, the cost of the dedicated PCMCIA card and the outboard assembly cable can constitute a significant portion of the total cost of the peripheral device. When the computer user adds another peripheral device to the computer capability, a separate dedicated PCMCIA card and outboard assembly cable specific to that device are purchased.

The present inventor has recognized a need for an improved approach to interfacing peripheral devices to computers, particularly portable computers. Such an interfacing approach would desirably reduce the cost of interfacing various types of peripheral devices to the computer, while managing the power requirements for the peripheral devices and the computer. The present invention fulfills this need, and further provides related advantages.

Disclosure of The Invention

The present invention provides an interfacing architecture and associated apparatus for interfacing a computer to a peripheral device. The interface approach of the invention reduces the cost of obtaining interfaces between the computer and various peripheral devices. The approach also benefits manufacturers of peripheral devices, because the interface structures can be developed more rapidly and less expensively than in the prior approach. Power isolation between the computer and the peripheral device is improved, reducing the

likelihood that power from the peripheral device can find its way into the computer.

In accordance with the invention, apparatus used to interface a peripheral device to a computer includes first means connectable to a computer for providing a reconfigureable interface circuit operable to reconfigure an interface bus according to flexibly defined signals between the computer and a peripheral device interface circuit. The apparatus further includes second means connectable to the first means and to the peripheral device for providing device-specific information to reconfigure the reconfigureable interface circuit of the first means and to provide the peripheral device interface circuit.

More specifically, apparatus used to interface a peripheral device to a computer comprises an adapter card including a reconfigureable interface circuit that is in communication with a computer when the adapter card is connected to the computer. There is an adapter card/computer connector configured to connect the adapter card to the computer. A portion of the adapter card/computer connector is in the computer and a portion of the adapter card/computer connector is in the adapter card. The apparatus further includes a smart cable having a first memory containing configuration information for the reconfigureable interface circuit. The first memory is accessible by the reconfigureable interface circuit when the smart cable is connected to the adapter card. There is a second memory containing adapter card information structure information for the reconfigureable interface circuit. The second memory is accessible by the reconfigureable interface circuit when the smart cable is connected to the adapter card. The apparatus further includes

a peripheral device interface circuit communicating with the reconfigureable interface circuit and with the peripheral device when the smart cable is connected to the adapter card and the peripheral device is connected to the smart cable. The apparatus includes a smart cable/adapter card connector configured to connect the smart cable to the adapter card. A portion of the smart cable/adapter card connector is in the adapter card and a portion of the smart cable/adapter card connector is in the smart cable. A peripheral device/smart cable connector is configured to connect the peripheral device to the smart cable, with a portion of the peripheral device/smart cable connector being in the smart cable and a portion of the peripheral device/smart cable connector being in the peripheral device.

The adapter card and the smart cable are each separate aspects of the invention in their own right. The adapter card has a fixed hardware structure and a reconfigureable electronic structure. The smart cable, on the other hand, is configured specifically for a particular peripheral device. That is, all of the device-specific aspects of the interface are found in the smart cable.

Brief Description of The Drawings

Figure 1 is a schematic diagram of the preferred architecture of the computer/peripheral interface;

Figure 2 is a pin configuration drawing for a preferred 23-pin bus connector between the adapter card and the smart cable;

Figure 3 is a schematic diagram of another embodiment of the computer/peripheral interface;

Figure 4 is a schematic drawing of a conventional computer/peripheral interface, with Figure 4A depicting the interface for a first peripheral device and Figure 4B depicting the interface for a second peripheral device; and

Figure 5 is a schematic drawing of the present computer/peripheral interface, with Figure 5A depicting the interface for a first peripheral device and Figure 5B depicting the interface for a second peripheral device.

Best Mode for Carrying Out The Invention

Figure 1 illustrates, in block diagram form, a preferred apparatus 20 used to interface a peripheral device 22 to a computer 24. The apparatus 20 includes an adapter card 26 which connects to the computer 24, and a smart cable 28 which connects between the adapter card 26 and the peripheral device 22.

The adapter card 26 has mounted thereon a reconfigureable interface circuit 30. The reconfigureable interface circuit 30 is preferably a reconfigureable PCMCIA (Personal Computer Memory Card International Association) card, interface chip, or circuit, and is most preferably a programmable gate array (PGA) chip or circuit. Such a PGA chip is available commercially as the Xilinx Programmable Gate Array Model XC3042. Briefly, the PGA circuit comprises a plurality of programmable gates, and the capability to automatically program or reconfigure the electronic circuitry of those gates utilizing information stored in accessible memories, upon command or powering of the chip. In effect, the circuit 30 acts as a programmable array of switches and other devices that serve to

interconnect specified pins of the connectors, specify the speed of the interface, identify which signals of the connectors serve as input, output, etc., and other programmable functions. All of the reconfigureable functions of the apparatus 20 are accomplished by the reconfigureable interface circuit 30, using specified configurations to be supplied in the manner described next.

The smart cable 28 has mounted thereon a first memory 32 containing configuration information for initially reconfiguring the reconfigureable interface circuit 30. This configuration information defines the bus interface, defines address decoding, provides the types of accessible cycles, provides the protocol for connection to the peripheral device interface circuit 36, and provides the logic for accomplishing these functions. The memory 32 is preferably a PROM (programmable read-only memory), and is most preferably a serially configured PROM. A serial PROM operable with the Xilinx reconfigureable interface circuit 30 is available as the Xilinx XC1765 serial configuration PROM. When the reconfigureable interface circuit 30 is powered, or otherwise commanded, it accesses the first memory 32 to obtain initial configuration information that causes the gates in the PGA circuit to reconfigure according to the contents of the first memory 32.

The smart cable 28 further has mounted thereon a second memory 34 containing card information structure (CIS) information that is used by the host computer 24 to interact with the peripheral device 22. Information such as the type of device, address mapping, interrupt capability, how to program any programmable memory, and also the access time information is provided by the second memory 34 to the computer 24, through the

programmable gate array of the reconfigureable interface circuit 30 as previously configured by reference to the first memory 32. That is, the information of the second memory 34 is not transmitted to the computer 24 until the reconfigureable interface circuit 30 has been configured properly for the particular peripheral device 22.

The first memory 32 and the second memory 34 may be provided on the same memory chip, but their functions are distinct. The first memory 32 contains information to initially configure or reconfigure the reconfigureable interface circuit 30. It is normally accessed by the reconfigureable interface circuit 30 only once, prior to any communication between the computer 24 and the peripheral device 22. The second memory 34 contains information that is repeatedly accessed by the computer 24 during communication with the peripheral device 22, and acts in the manner of an extension of the computer's memory as specifically related to the peripheral device. Faster access to the second memory 34 than to the first memory 32 is therefore required in most instances. The second memory 34 is preferably a parallel-configured PROM, such as an AMD AM27C64 one-time programmable memory.

The smart cable 28 further includes a peripheral device interface circuit 36 that communicates between the reconfigureable interface circuit 30 and the peripheral device 22. The peripheral device interface circuit 36 is a standard circuit or chip for the peripheral device 22. Thus, for example, the circuit 36 may be a Rockwell 224ATF for a modem, a National Semiconductor ST-NiC chip for a local area network, or an Adaptec AIC-6260 chip for SCSI interface. These circuits are routinely provided by semiconductor manufacturers to

drive various standard peripheral devices 22. Such a peripheral device interface circuit 36 requires particular inputs, outputs, timing signals, and other information to and from the computer 24. The nature and locations of the chip inputs and outputs and the necessary interface reconfiguration are stored in the memories 32 and 34 for use in the manner previously discussed.

The adapter card 26 (and thence the reconfigureable interface circuit 30) is connected to the computer 24 with an adapter card/computer connector 38. The nature of this connector is dictated by the port configuration of the computer 24. In the preferred form of the invention, the adapter card 26 is connected to the PCMCIA socket of the computer. In currently available portable computers, the PCMCIA socket normally has a 68-pin connector, and therefore the connector 38 is a 68-pin connector. A portion of the connector 38 (either the male or the female portion) is located in the computer 24, and the other portion is located in the adapter card 26 for quick connection and disconnection of the adapter card 26 and the computer 24.

The smart cable 28 (and thence the memories 32 and 34 and the peripheral device interface circuit 36) is connected to the adapter card 26 (and thence the reconfigureable interface circuit 30) by a smart cable/adapter card connector 40. this connector 40 is preferably a 23-pin connector configured as shown in Figure 2. Three pin locations are used as guide pins, five pins have predefined functions (ground, clock, data, voltage, reconfiguration command), and the remaining pins (labelled I/O) are fully programmable according to the configuration established in the programming of the reconfigureable interface circuit 30. These

programmable pins are not programmed arbitrarily, but are programmed according to the input/output requirements of the peripheral device interface circuit 36. These requirements and pin assignments are stored in the first memory 32 and serve as part of the information that is used to initially reconfigure the circuit 30. Thus, they cannot be specified herein in any general sense, as their function will vary according to the specific peripheral device for which the interface apparatus 20 is configured.

The peripheral device 22 is connected to the smart cable 28 (and thence the peripheral device interface circuit 36) by a peripheral device/smart cable connector 42. This connector will be of any type required by the peripheral device. As discussed earlier, examples include an RJ-11 connector for a modem, an RJ-45 connector for a local area network, or a 50-pin Centronics connector for a SCSI interface.

An alternative structure of the apparatus 20 is illustrated in Figure 3. Here, the majority of the components are identical to those shown in Figure 1, and are numbered identically. These components function as previously described, except as next discussed. The apparatus 20 of Figure 3 substitutes a slower serial CIS PROM for the parallel CIS PROM of the second memory 34. To compensate for the slower access times for information transferred from the second memory 34 to the computer 24 inherent in this arrangement, a random access memory (RAM) 44 is added to the adapter card 26. During the initial configuration, the information in the second memory 34 is transferred to the random access memory 44 on the adapter card 26. The memory 44 is accessible by the reconfigureable interface circuit 30, which is

configured to supply from the memory 44 the information originally found in the second memory 34. The access of the computer 24 to the information in the second memory 34 is therefore not slowed by the serial nature of the second memory 34. In addition, the unused portion of the RAM 44 may be used for other purposes as defined by the configuration of the reconfigureable interface circuit 30, the program or device driver of the computer 24, and the functionality of the peripheral device integrated circuit 36. These other uses include a FIFO buffer between the computer 24 and the peripheral device interface circuit 36, a DMA buffer for the peripheral device interface circuit 36, or a scratch-pad memory for the computer 24.

The principal functional differences between the prior conventional approach and the present approach are depicted in Figures 4 and 5. Figure 4, the conventional approach, shows a device-specific PCMCIA card 50 that is plugged into the computer 24. (The term "device-specific" means that the structure can be used only with a specific type of peripheral device, and not with other peripheral devices.) A device-specific cable 52 (i.e., a dongle) with outboard electronics assembly is connected at one end to the card 50 and at the other end to the peripheral device 22. In Figure 4A, a particular peripheral device 22 is used, and device-specific cards 50 and cable 52 are required. If another peripheral device 22' is substituted for the peripheral device 24, as shown in Figure 4B, then an entirely new device-specific PCMCIA card 50' and device-specific cable 52' must be obtained and used.

By contrast, the present approach is shown in Figure 5. A single, common (universal) adapter card 26 is plugged into the computer 24, regardless of

whether the peripheral device 22 (Figure 5A) or the peripheral device 22' (Figure 5B) is selected. Only the smart cable 28 is changed. A first device-specific smart cable 28 is supplied and used for the peripheral device 24 (Figure (5A) and a second device-specific smart cable 28' is supplied and used for the peripheral device 24' (Figure 5B).

The increased commonality and reduced cost of a universal adapter card 26 operable with all peripheral devices is apparent. If the user has more than one peripheral device, the total product cost is reduced because only one adapter card need be purchased. Other associated advantages of the present approach over the prior approach are less apparent but equally important. The manufacturers of peripheral devices need not design a new device-specific card 50 for each new product or product improvement. The adapter card remains physically unchanged, but the reconfigureable interface circuit is reconfigured for each peripheral device or modification by providing different information in the memories 32 and 34. Providing this information in memory is a less complex, less costly, and more quickly accomplished task than redesigning and debugging a new device-specific PCMCIA card 50 for each new product. Thus, product development costs of the manufacturer are reduced, and product introduction or upgrade times are reduced.

The present approach also more effectively isolates the internal circuitry of the computer from the internal circuitry of the peripheral device and its peripheral device interface circuit. In some instances, the peripheral devices and their peripheral device interface circuits require more power than a portable computer can reasonably provide without excessive battery drain. The power

to operate the peripheral device and its interfacing circuitry must be provided by an external power supply. If the voltages in the external power supply are introduced into the circuitry within the computer, the computer circuitry may be damaged, or operations may be disrupted. The prior architecture of Figure 4, with the card 50 directly connected to the computer through the 68-pin connector, may result in such leakage of voltage levels of the external power supply into the internal circuitry of the computer. In the present approach, however, the smart cable/adapter card connector 40 and the reconfigureable interface circuit 30 effectively isolate voltages of an external power supply from the computer 24.

Although a particular embodiment of the invention has been described in detail for purposes of illustration, various modifications may be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be limited except as by the appended claims.

CLAIMS

1. Apparatus used to interface a peripheral device to a computer, comprising:

an adapter card including a reconfigureable interface circuit that is in communication with a computer when the adapter card is connected to the computer;

an adapter card/computer connector configured to connect the adapter card to the computer, a portion of the adapter card/computer connector being in the computer and a portion of the adapter card/computer connector being in the adapter card;

a smart cable including

a first memory containing configuration information for the reconfigureable interface circuit, the first memory being accessible by the reconfigureable interface circuit when the smart cable is connected to the adapter card,

a second memory containing adapter card information structure information for the reconfigureable interface circuit, the second memory being accessible by the reconfigureable interface circuit when the smart cable is connected to the adapter card, and

a peripheral device interface circuit communicating with the reconfigureable interface circuit and with the peripheral device when the smart cable is connected to the adapter card and the peripheral device is connected to the smart cable;

a smart cable/adapter card connector configured to connect the smart cable to the adapter card, a portion of the smart cable/adapter card connector being in the adapter card and a portion of the smart cable/adapter card connector being in the

smart cable; and

a peripheral device/smart cable connector configured to connect the peripheral device to the smart cable, a portion of the peripheral device/smart cable connector being in the smart cable and a portion of the peripheral device/smart cable connector being in the peripheral device.

2. Apparatus used to interface a peripheral device to a computer, comprising an adapter card including

a reconfigureable interface circuit that is in communication with a computer when the adapter card is connected to the computer;

a portion of an adapter card/computer connector configured to connect the adapter card to the computer; and

a portion of a smart cable/adapter card connector configured to connect a smart cable to the adapter card.

3. The apparatus of claim 1 or 2, wherein the reconfigureable interface circuit is a reconfigureable PCMCIA interface chip.

4. The apparatus of claim 1 or 2, wherein the reconfigureable interface circuit is a programmable gate array.

5. The apparatus of claim 1 or 2, wherein the adapter card further includes

a memory accessible by the reconfigureable interface circuit.

6. The apparatus of claim 1 or 2, wherein the adapter card/computer connector is a 68-pin connector.

7. Apparatus used to interface a peripheral device to a computer, comprising a smart cable including

a first memory containing configuration information for a reconfigureable interface circuit, the first memory being accessible by an external reconfigureable interface circuit when the smart cable is connected to the external reconfigureable interface circuit;

a second memory containing adapter card information structure information for the external reconfigureable interface circuit, the second memory being accessible by the reconfigureable interface circuit when the smart cable is connected to the external reconfigureable interface circuit;

a peripheral device interface circuit communicating with the reconfigureable interface circuit and with a peripheral device when the smart cable is connected to the reconfigureable interface circuit and the peripheral device is connected to the smart cable;

a portion of a smart cable/adapter card connector configured to connect the smart cable to an adapter card upon which the reconfigureable interface circuit resides; and

a portion of a peripheral device/smart cable connector configured to connect the peripheral device to the smart cable.

8. The apparatus of claim 1 or 7, wherein the first memory is a serial-configuration memory.

9. The apparatus of claim 1 or 7, wherein the second memory is a serial-configuration memory.

10. The apparatus of claim 1 or 7, wherein

the smart cable/adapter card connector is a 23-pin connector.

FIG. 2

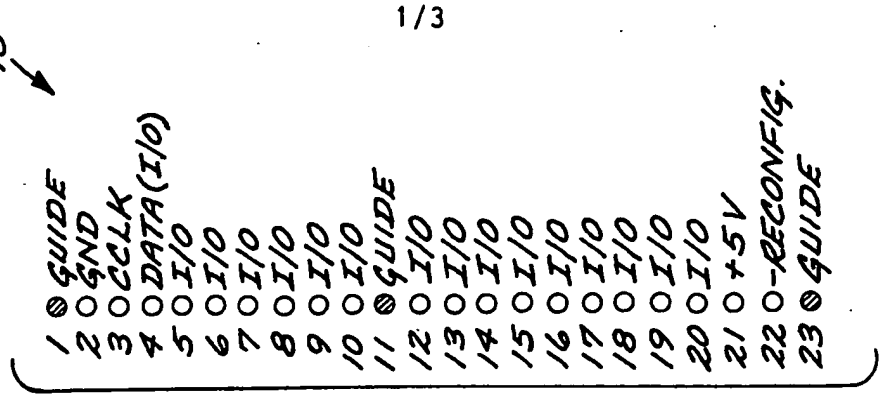


FIG. 1

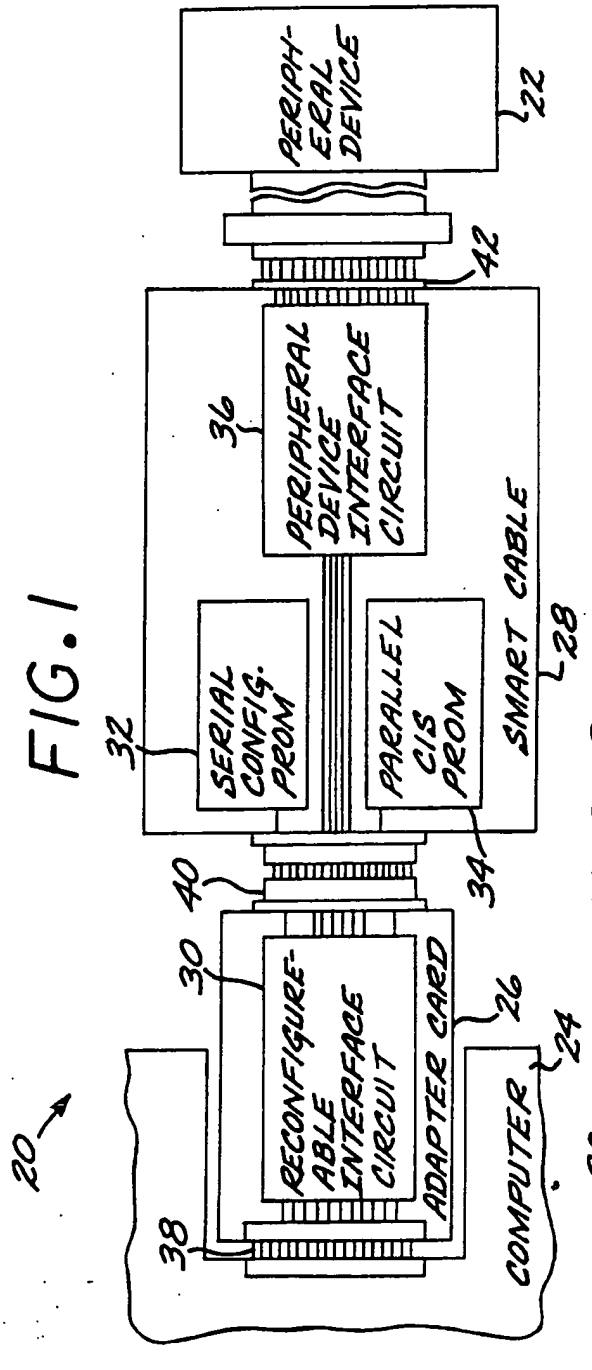
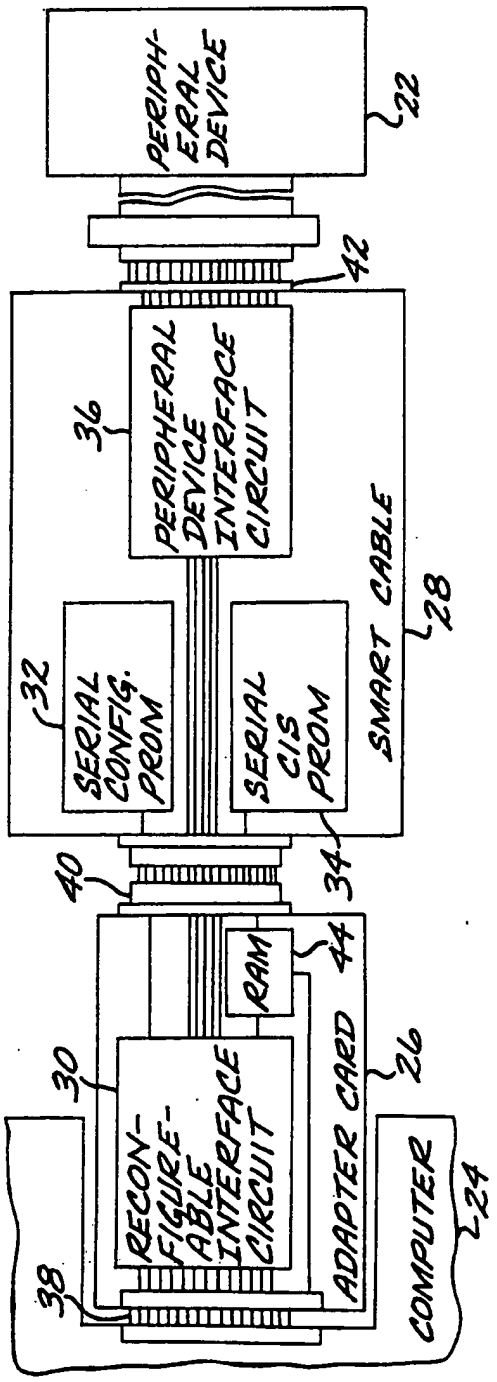


FIG. 3



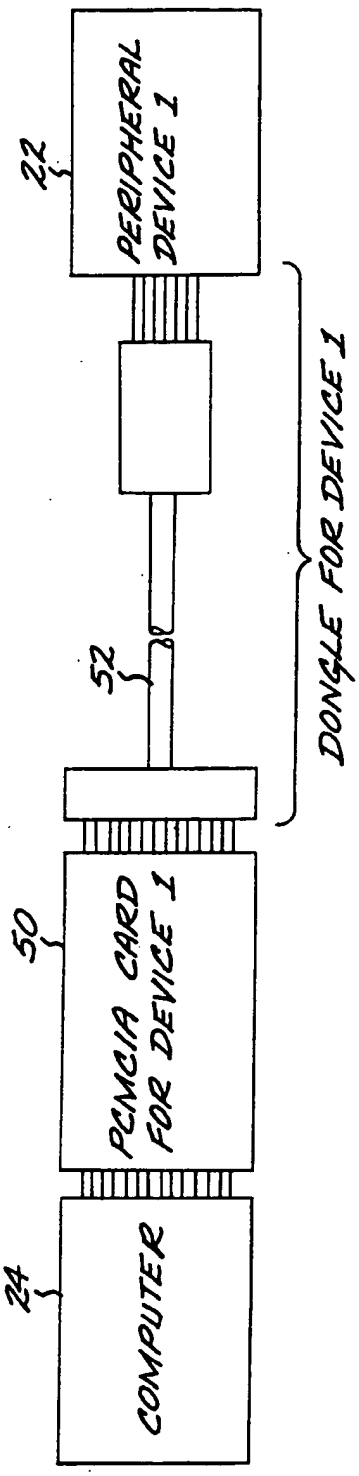
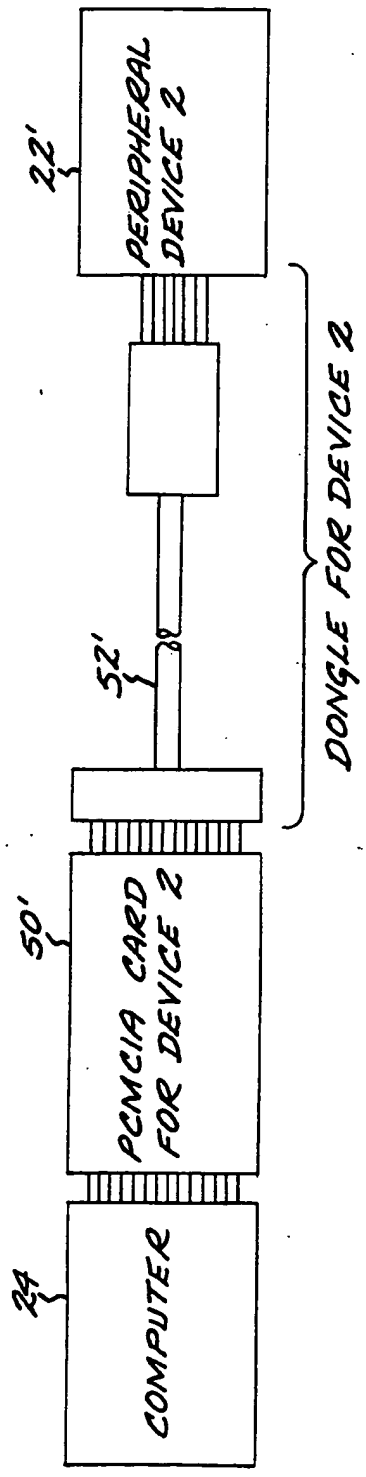

22
PERIPHERAL DEVICE 1
52
DONGLE FOR DEVICE 1
50
PCMCIA CARD FOR DEVICE 1
24
COMPUTER

FIG. 4A


22'
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52'
DONGLE FOR DEVICE 2
50'
PCMCIA CARD FOR DEVICE 2
24
COMPUTER

FIG. 4B

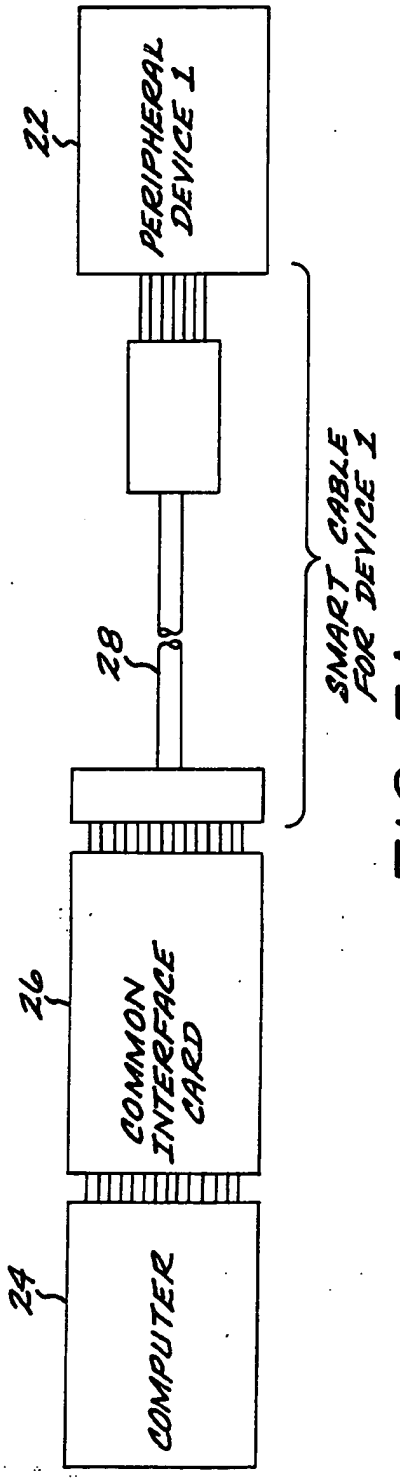
22
PERIPHERAL DEVICE 1
28
SMART CABLE FOR DEVICE 1
26
COMMON INTERFACE CARD
24
COMPUTER

FIG. 5A

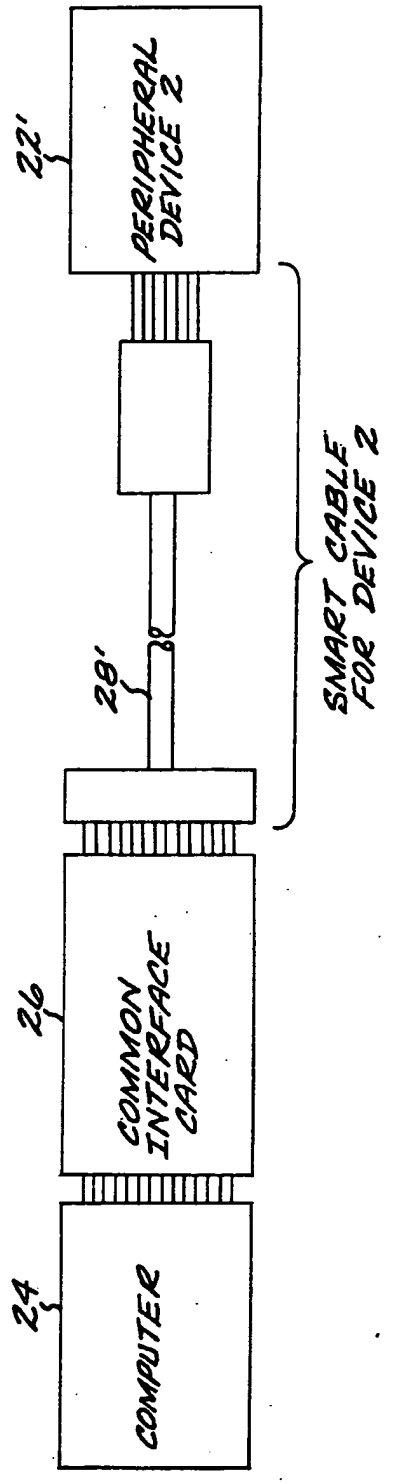
22'
PERIPHERAL DEVICE 2
28'
SMART CABLE FOR DEVICE 2
26
COMMON INTERFACE CARD
24
COMPUTER

FIG. 5B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/10845

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :G06F 3/00, 13/00, 13/38, 9/06; H05K 7/10
US CL :395/325, 275; 370/85.1; 340/825.06; 439/59; 361/395
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/325, 275; 370/85.1; 340/825.06; 439/59; 361/395

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS Search Terms: computer#, interfac?, peripheral#, I(w)O, adapter#, board#, card#, cable#, communication, reconfig?

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
y	US, A 5,101,481 (Anger et al) 31 March 1992 (31.03.92) Note: (see Fig. 1 and col. 2, line 38 - col. 3, line 5)	1-10
y	US, A 4,589,063 (Shah et al) 13 May 1986 (13.05.86) Note: (see Fig. 2 and col. 2, lines 7-42)	1-10
y	US, A 5,070,477 (Latif et al) 03 December 1991 (03.12.91) Note: (see Fig. 2 and col. 2, lines 18-45)	1-10

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	Authorized officer GOPAL C. RAY
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/10845

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
y	US, A 4,504,927 (Callan) 12 March 1985 (12.03.85) Note: (see Figures 2-3 and col. 1, line 54 - col. 2, line 12)	1-10
y,p	US, A 5,179,628 (Muranoi) 12 January 1993 (12.01.93) Note: (see Fig. 1 and col. 2, lines 25-61)	1-10
y	US, A 3,828,326 (Cash) 06 August 1974 (06.08.74) Note: (see Fig. 1 and col. 2, lines 15-48)	1-10
y	US, A 4,941,089 (Fischer) 10 July 1990 (10.07.90) Note: (see Figures 1-8 and col. 2, line 56 - col. 3, line 35)	1-10
y,p	US, A 5,163,833 (Olsen et al) 17 November 1992 (17.11.92) Note: (see Figures 1 and 12; col. 2, line 29 - col. 3, line 66)	1-10
y,p	US, A 5,187,645 (Spalding et al) 16 February 1993 (16.02.93) Note: (see col. 1, lines 24-55)	1-10
y	Xilinx Corp., "The Programmable Gate array Data Book", pages 2-1 to 2-26 (1991) Note: (see page 2-1)	4
y	Kenneth K. Hillen et al, "Build Reconfigurable Peripheral controllers", Electronic Design (March 1990), pages 7-1 to 7-7 Note: (see pages 7-1 to 7-3)	4